APRIL: a processor architecture for multiprocessing

Agarwal, A. Lim, B.-H. Kranz, D. Kubiatowicz, J.
Lab. for Comput. Sci., MIT, Cambridge, MA, USA;
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Abstract:
The architecture of a rapid-context-switching processor called APRIL, with support for fine-grain threads and synchronization, is described. APRIL achieves high single-thread performance and supports virtual dynamic threads. A commercial reduced-instruction-set-computer-(RISC-) based implementation of APRIL and a run-time software system that can switch contexts in about 10 cycles are described. Measurements taken for several parallel applications on an APRIL simulator show that the overhead for supporting parallel tasks based on futures is reduced by a factor of 2 over a corresponding implementation on the Encore Multimax. The scalability of a multiprocessor based on APRIL is explored using a performance model. The authors show that the SPARC-based implementation of APRIL can achieve close to 80% processor utilization with as few as three resident threads per processor in a large-scale cache-based machine with an average base network latency of 55 cycles

Index Terms:
parallel architectures parallel machines synchronisation APRIL Encore Multimax SPARC-based implementation cache-based machine fine-grain threads network latency rapid-context-switching processor synchronization virtual dynamic threads